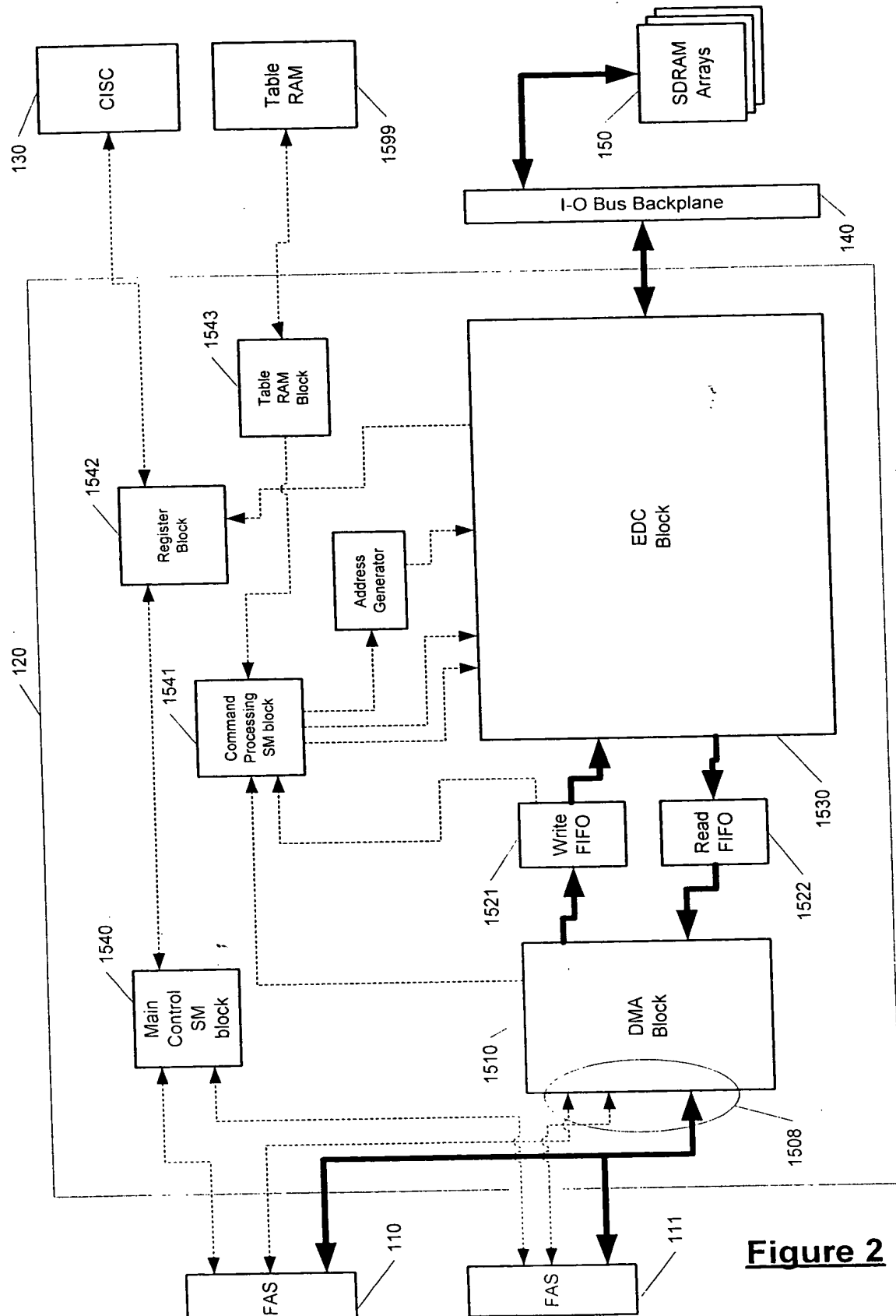
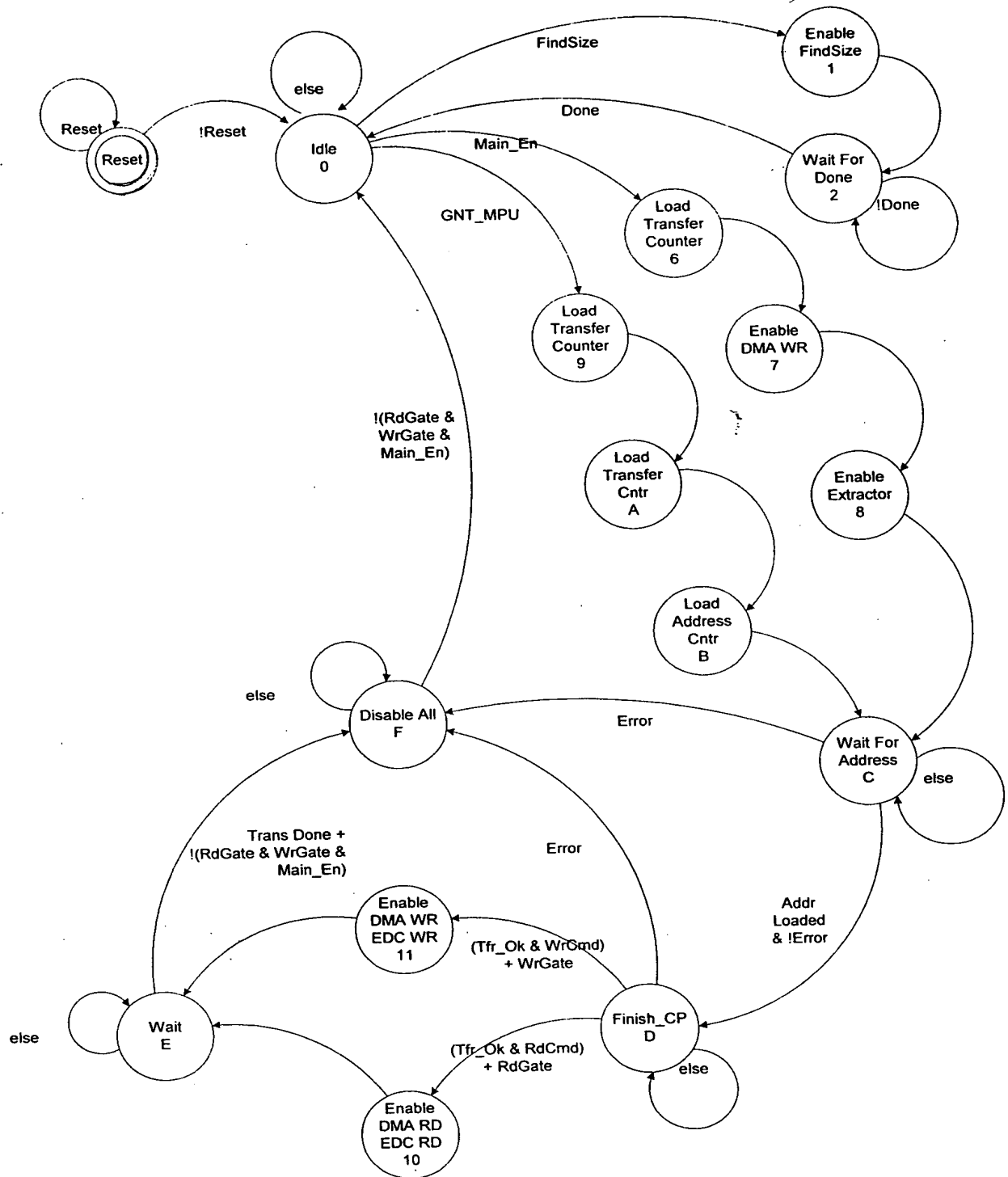


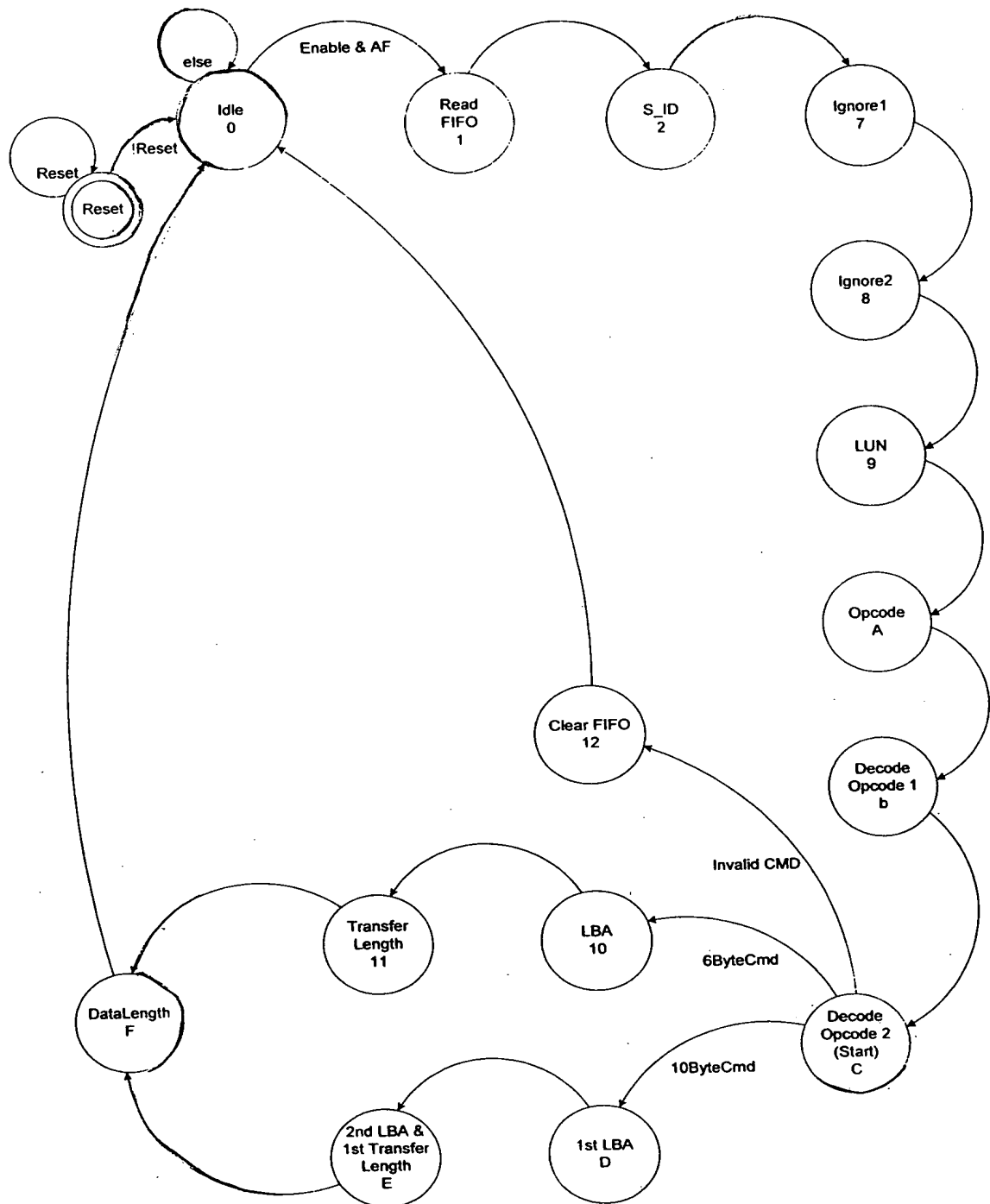
Figure 1

**Figure 2**



Main State Diagram

Figure 3



Extractor State Diagram

Figure 4

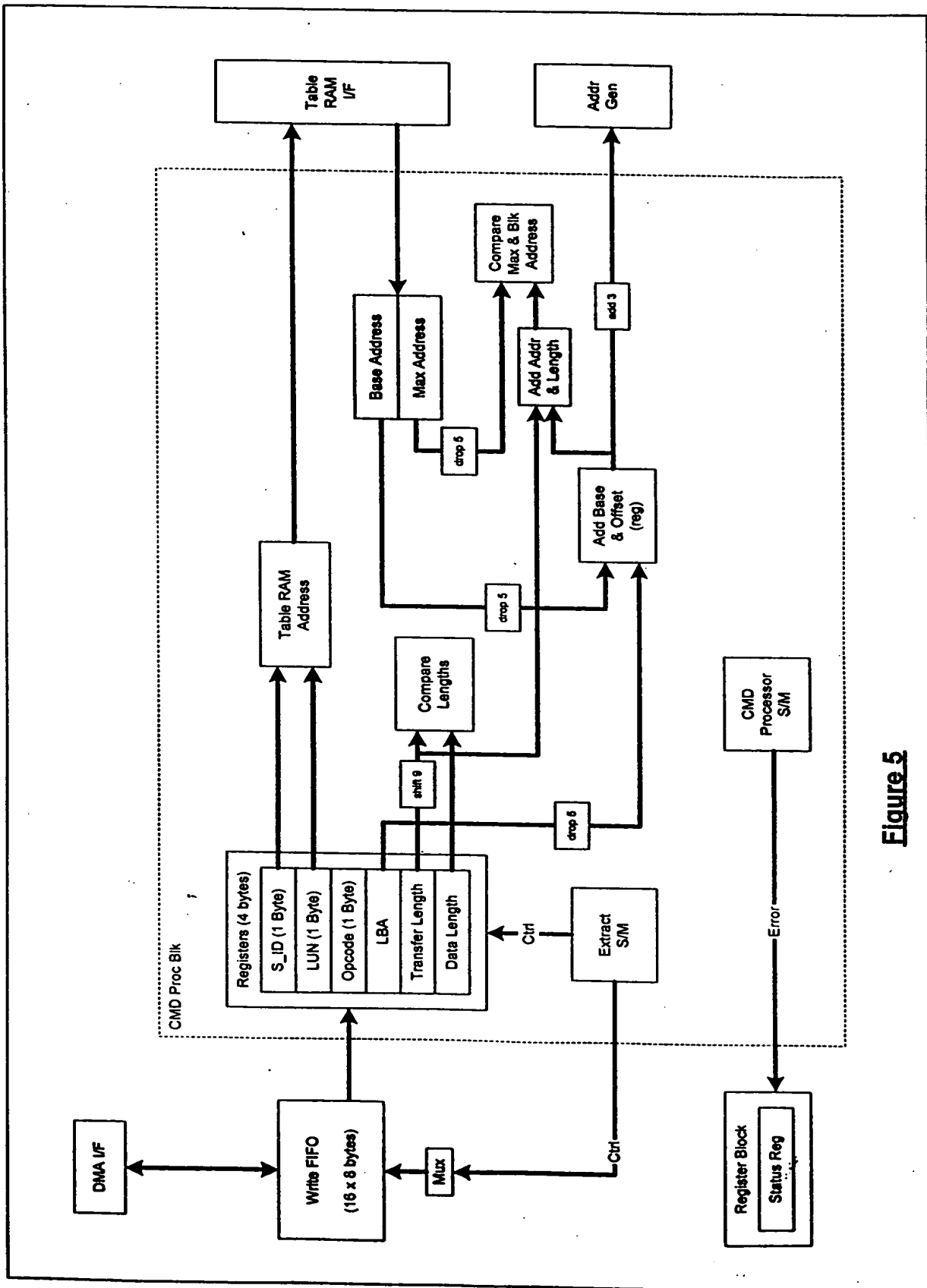
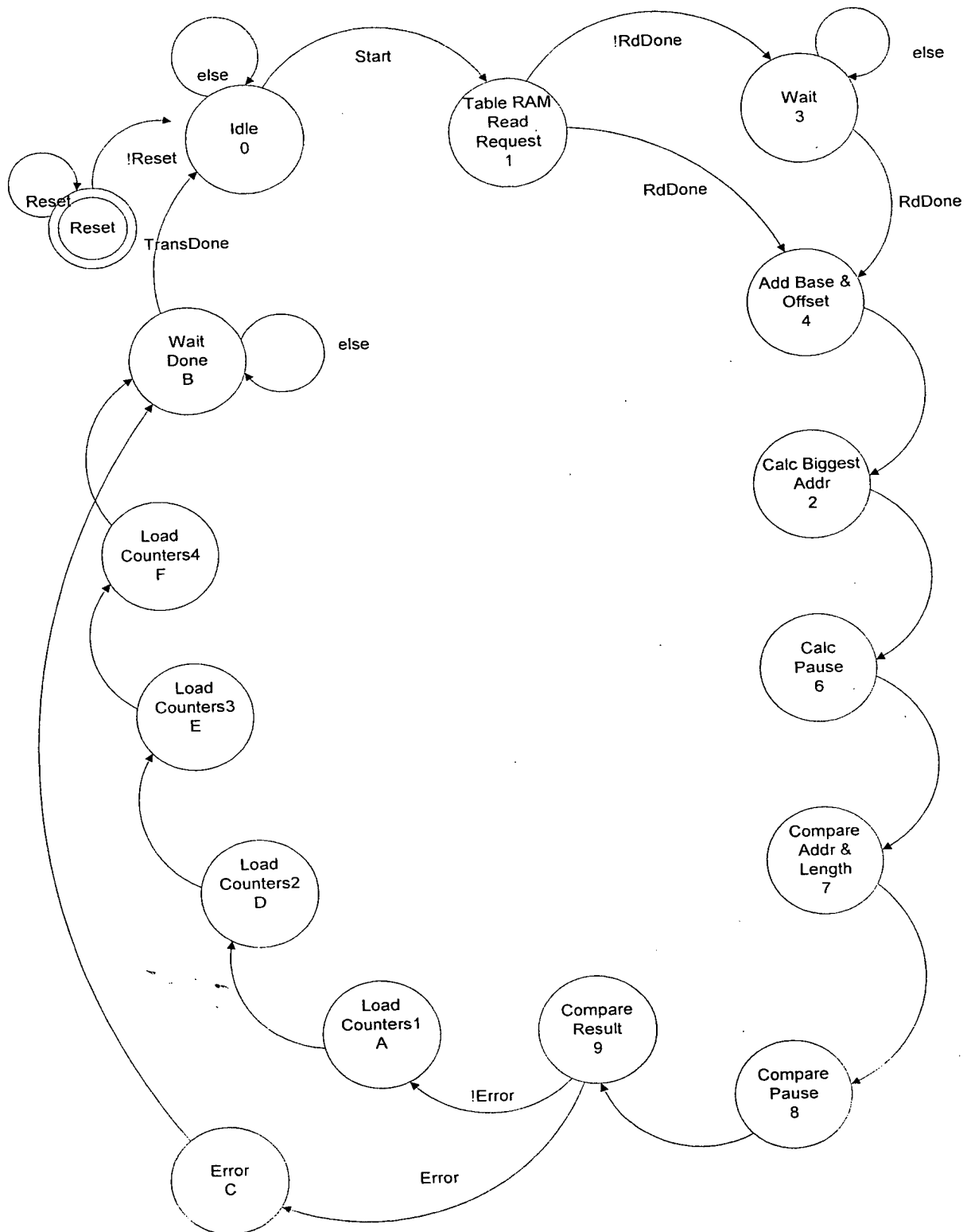
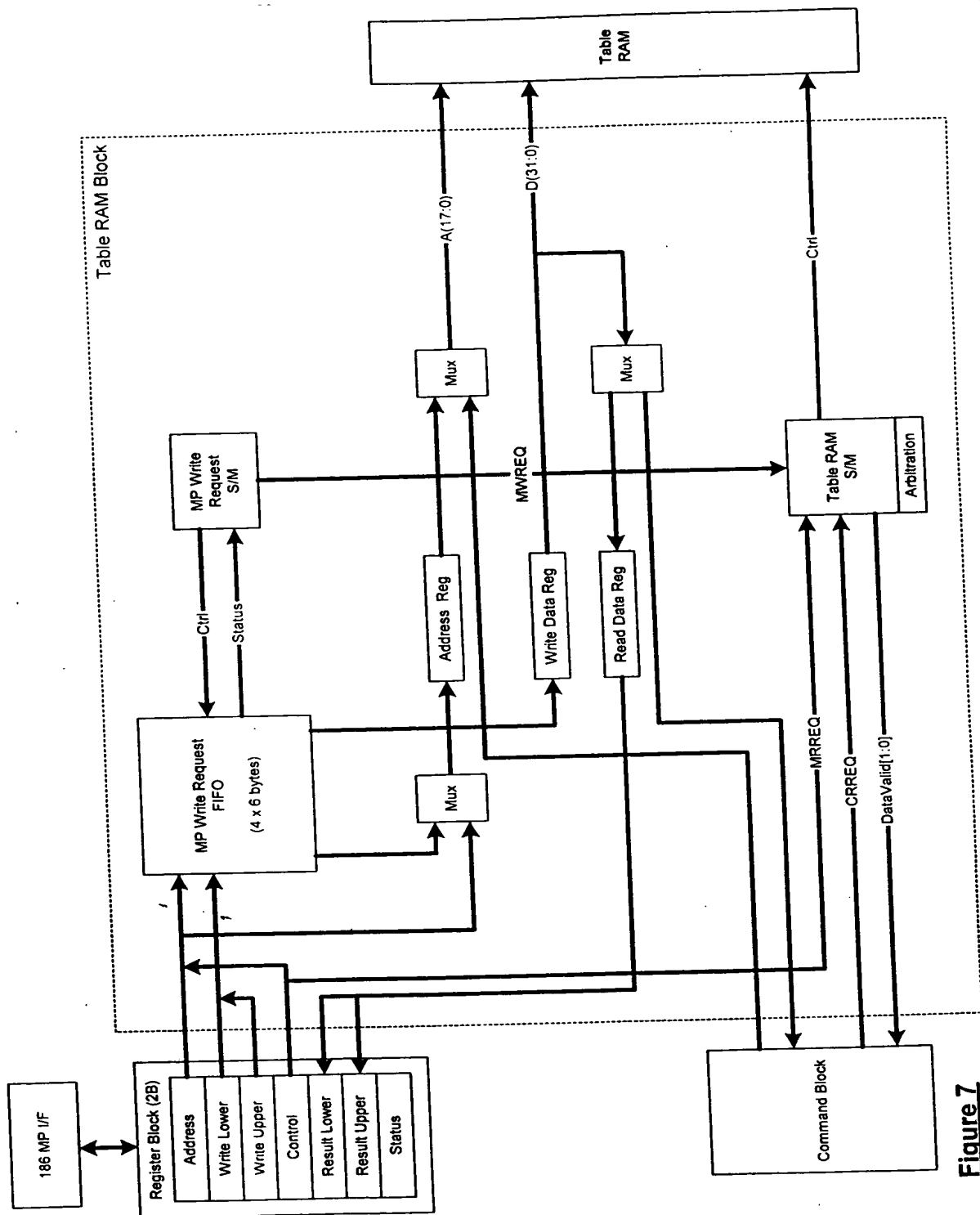
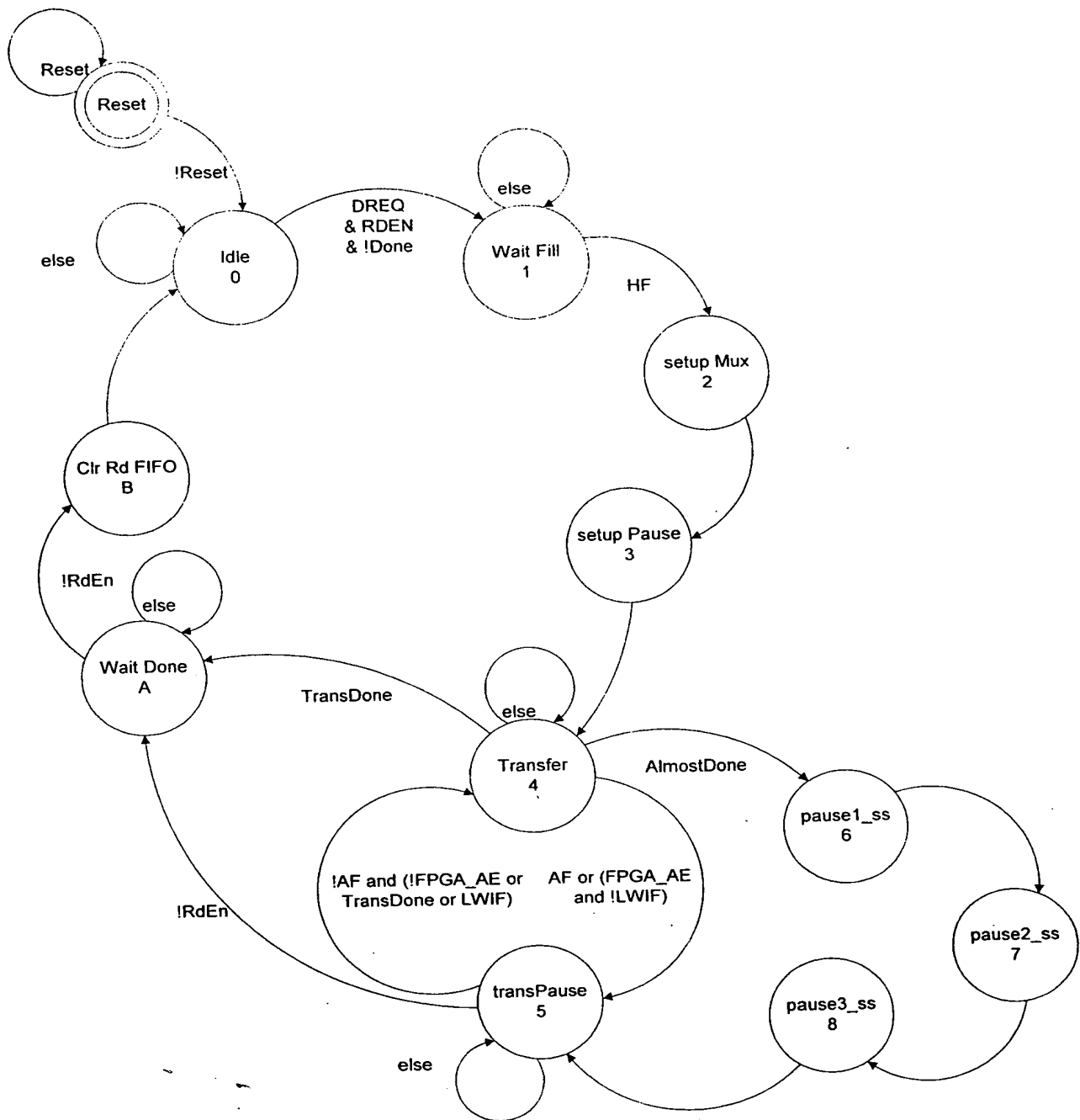


Figure 5

**Figure 6**

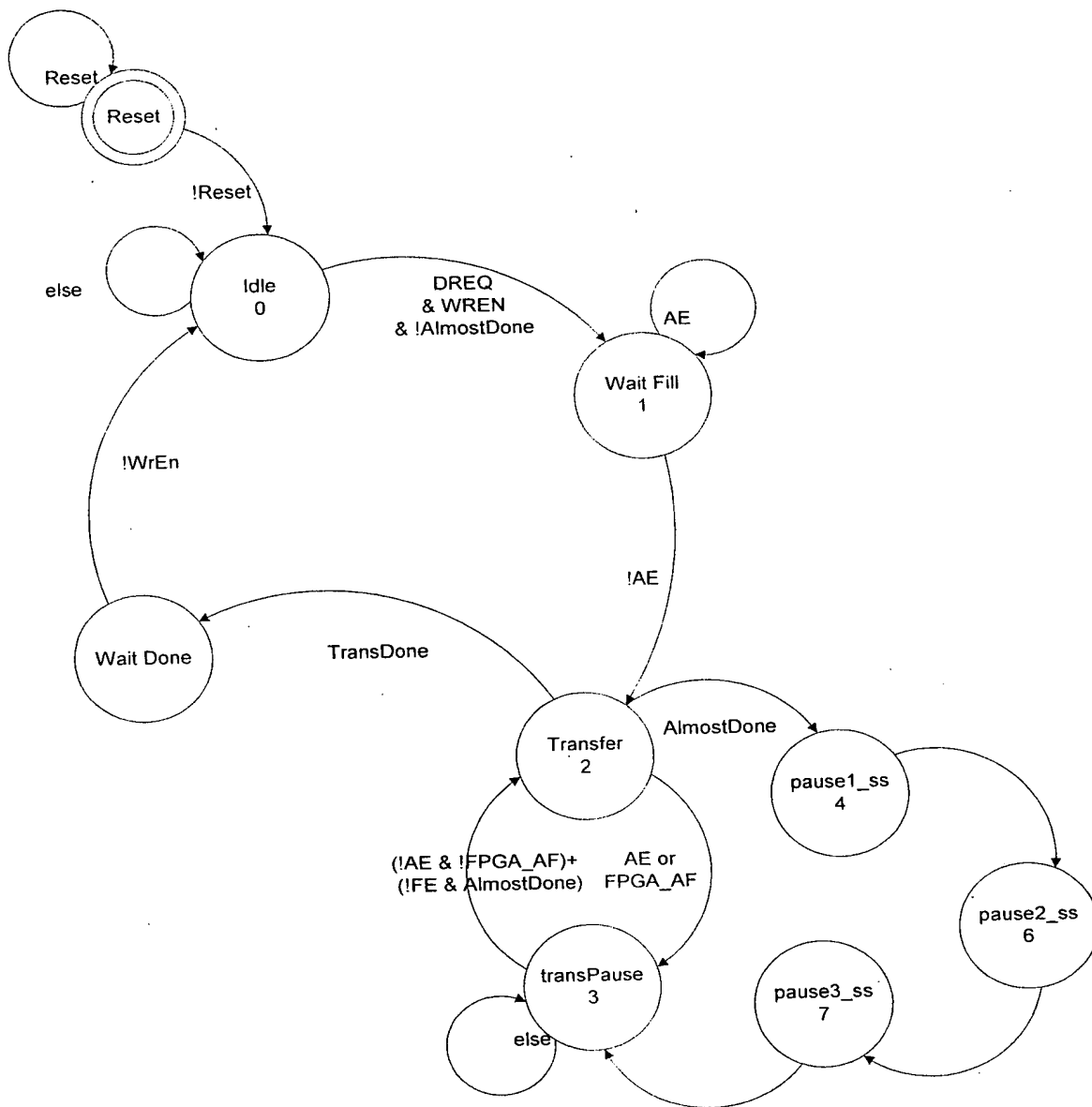
CMD Processor State Diagram

**Figure 7**



DMA Read State Diagram

Figure 8



DMA Write State Diagram

Figure 9

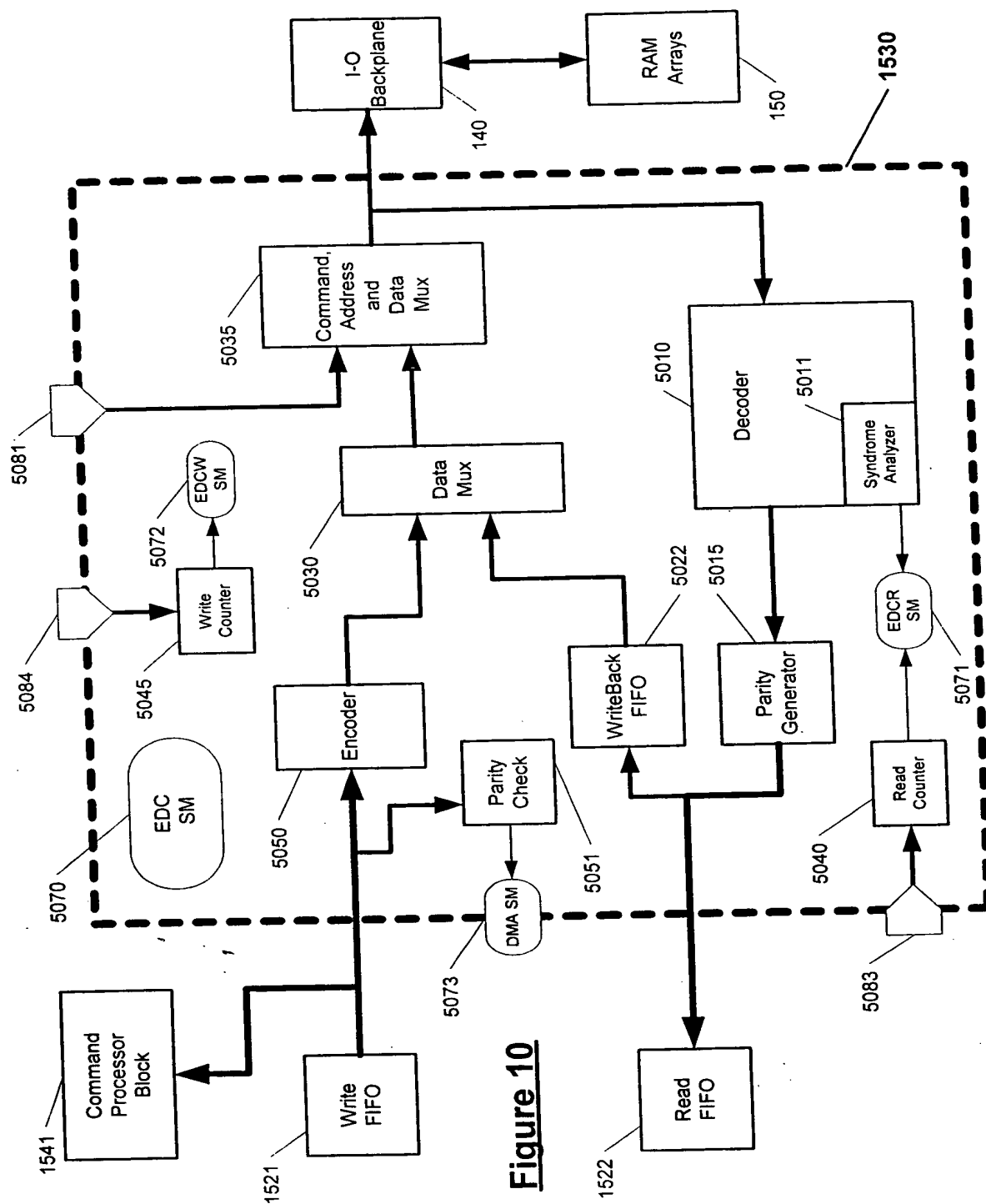
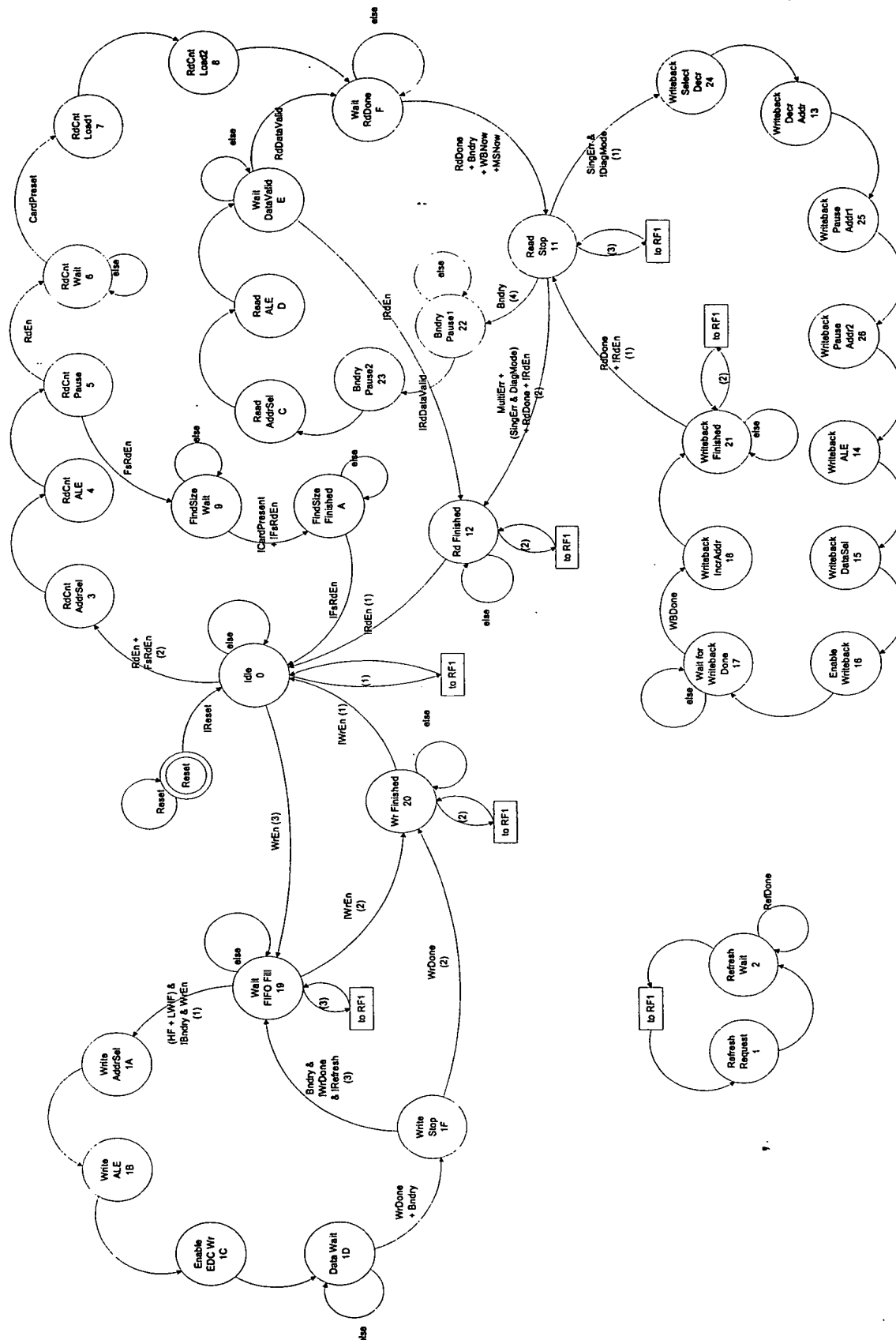
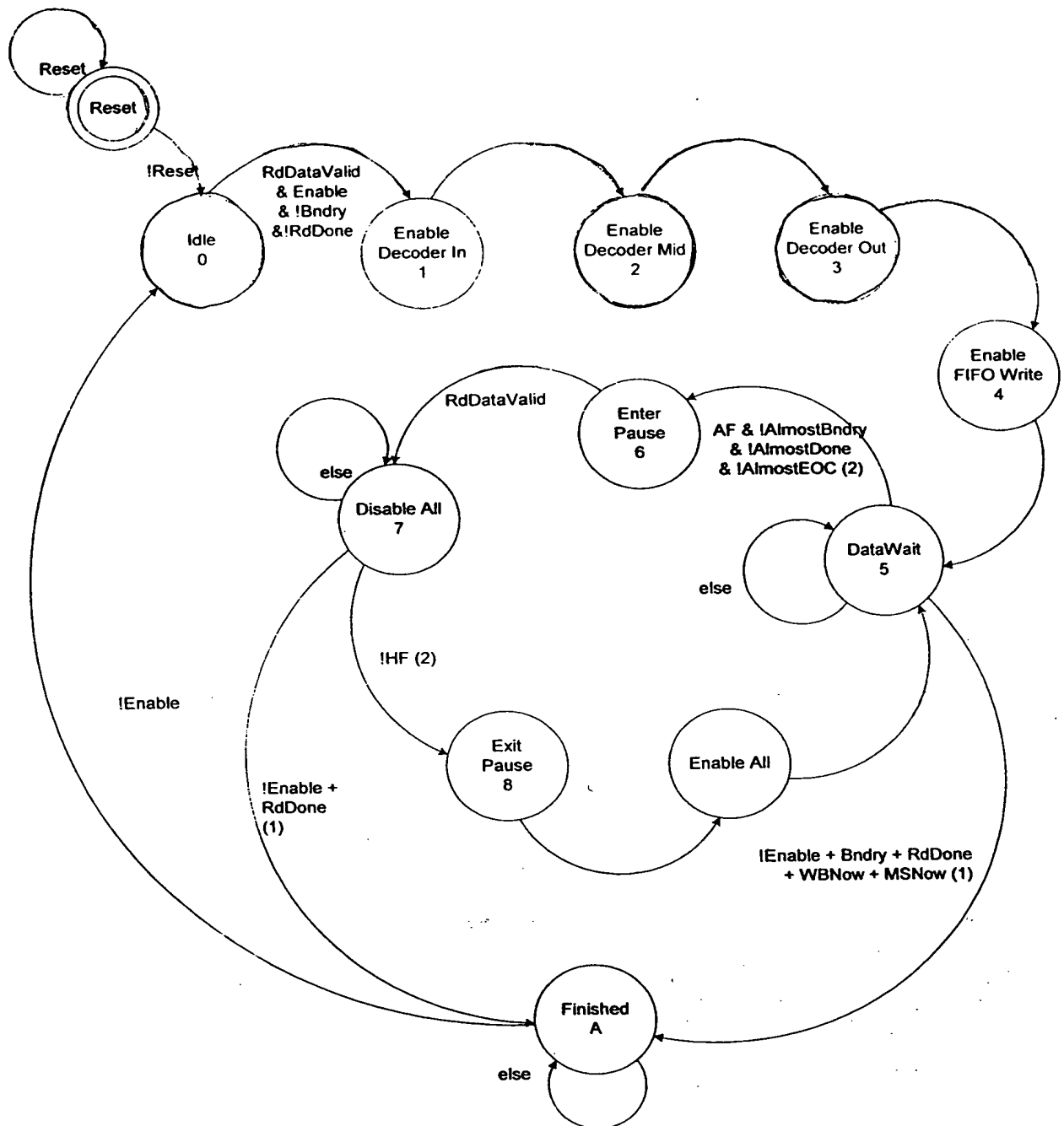


Figure 10



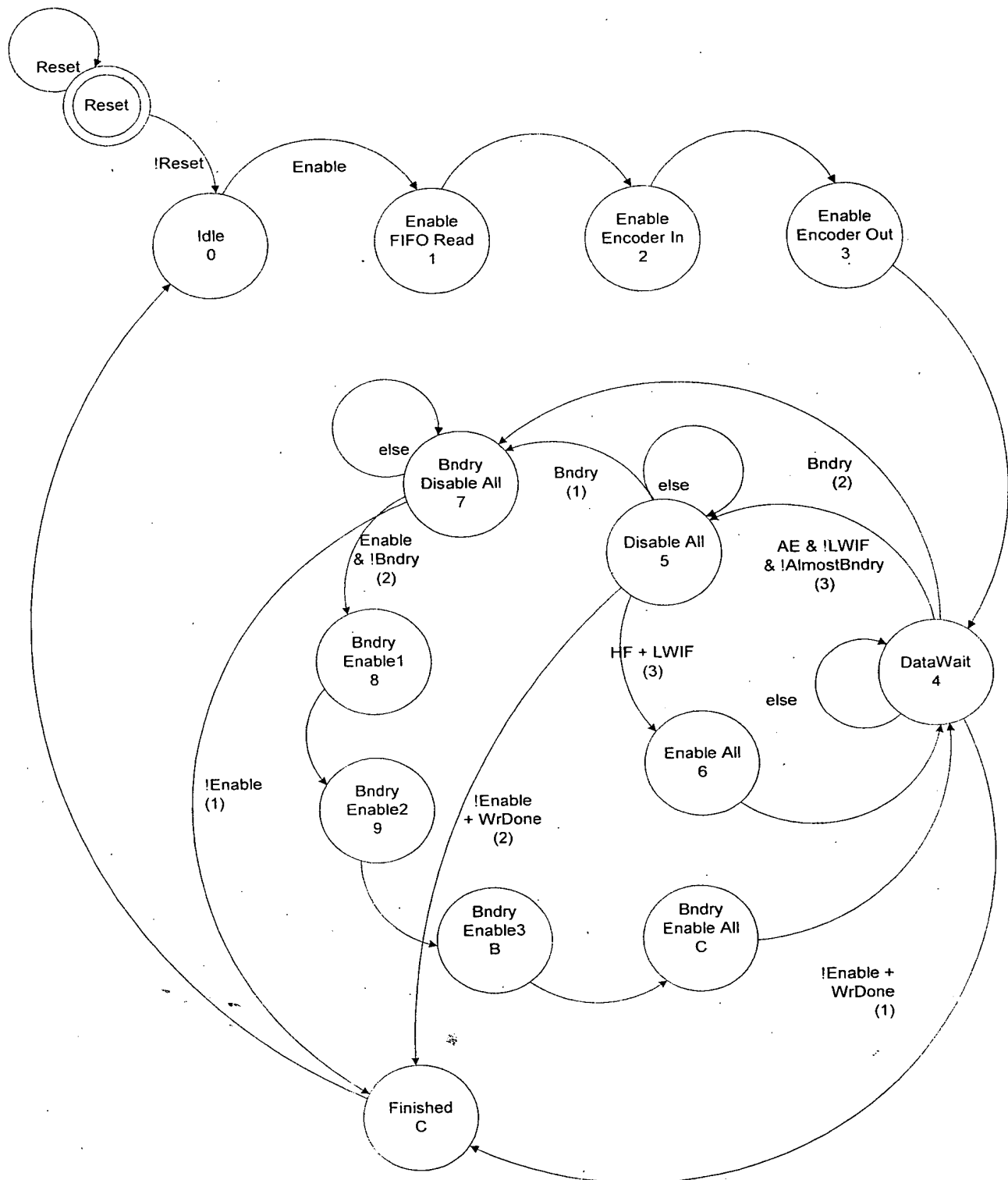
EDC State Diagram

FIGURE 11



EDC Read State Diagram

Figure 12



EDC Write State Diagram

Figure 13